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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,478	03/23/2004	Raminderpal Singh	FIS920040073US1	3056

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EXAMINER	
WHITMORE, STACY	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H9

Office Action Summary	Application No.	Applicant(s)	
	10/807,478	SINGH ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,10,11,15 and 17* is/are rejected.

7)☒ Claim(s) *2,6-9,12-14 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 3-5, 10, and 17 rejected under 35 U.S.C. 102(b) as being anticipated by Lampaert (US Patent Application Publication 2002/0188920).

2. As for the following claims, Lampaert discloses the invention substantially as claimed, including:

1. and 17. A program storage device readable by a machine, tangibly embodying a program o: instructions executable by the machine to perform a method of performing a physical verification of the layout of an integrated circuit comprising the steps of:
identifying transistors in a sub-circuit configuration that includes respective interconnections linked to each of said transistors [abstract, paragraph 0055, 0057, fig. 6];
measuring parameters of each of said sub-circuits [paragraphs 0055-0057 – the predictive RF MOSFET layout is an extraction];
comparing the measured parameters of each of said sub-circuits against corresponding parameters of a schematic netlist [fig. 8, element 810], and
determining if all of said comparisons returns a correct correlation paragraph 0066 - LVS], and

reporting when any of said comparisons returns a mismatched correlation [paragraph 0066 – DRC and LVS identify violations between the layout and schematic].

3. The method of claim 1, wherein said transistor in said layout is a single fingered field-effect transistor (FET) [paragraph 0016, 0032].

4. The method of claim 1, wherein said transistor in said layout is a multi-fingered field-effect transistor (FET) [paragraph 0016, 0032].

5. The method of claim 4, wherein the measured parameters of said multi-fingered transistor are respectively compared to corresponding parameters of said schematic netlist [fig. 8, element 810, paragraph 0066 – DRC and LVS identify violations between the layout and schematic].

10. The method of claim 1, wherein said comparison of the measured parameters of each of said sub-circuits against the corresponding parameters of the schematic netlist further comprises comparing the diffusion dimensions of the source and the drain of said transistor to said schematic netlist [fig. 8, element 810, paragraph 0066 – DRC and LVS identify violations between the layout and schematic, paragraph 0032, diffusion dimensions].

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the

United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 11, and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Li (US Patent Application Publication 2004/00225125).

4. As for the following claims, Li discloses the invention as claimed, including:

11. A method for creating a device layout comprising the steps of:
providing device model parameters that support an extraction of a list of device layout geometric parameters [paragraph 0006 – "design layout describes the detailed design geometries; paragraph 0008 - extraction]; and
providing specific marker shapes to define the device layout geometric parameters [paragraph 0092 – marker geometries].
15. The method of claim 11, wherein further marker shapes are added to non-FET devices to perform a sub-circuit based extraction [paragraph 0043].

5. Claims 2, 6-9, and 12-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to discloses either singularly or in combination the invention as claimed, including a method of performing physical verification of a layout comprising at least the steps of: 2. The method of claim 1, wherein if said transistor is identified as a sub-circuit, then said comparison is performed in a sub-circuit extraction mode; otherwise, said comparison is performed by way of a flat extraction mode.
6. The method of claim 4, wherein said FET transistor comprises at least two gate regions shorted to each other, at least one drain and two source diffusion regions, said

two source diffusion regions being shorted to each other, or at least one source and two drain diffusion regions, said two drain diffusion regions being shorted to each other.
7. The method of claim 6, wherein said layout includes first marker shapes to identify said source or drain diffusion regions between pairs of said FET gate regions.
8. The method of claim 7, wherein said layout includes second marker shapes to identify said source or drain diffusion regions occurring outside said pairs of FET gate regions.
9. The method of claim 8, wherein said first and second marker shapes are used to form a netlist for said FET transistor.
12. The method of claim 11, wherein said model parameters comprise the channel length (L), finger width (WF), number of fingers (NF), left diffusion length (DIFFL), middle diffusion length (DIFFM), and right diffusion length (DIFFR) of an FET transistor.
13. The method of claim 12, wherein a minimum set of three FET transistor marker shapes (LEFT, MULTI, and RIGHT) are used for bulk Si and SOI technologies.
14. The method of claim 11, wherein said devices are selected from the group consisting of bipolar junction transistors (BJT), hetero-junction bipolar transistors (HBT), and compounded semiconductor transistors;
16. The method of claim I 5, wherein non-FET devices are selected from the group consisting of integrated on-chip inductors, integrated on-chip capacitors, resistors, and varactors.

Applicant's arguments filed January 17, 2006 have been fully considered but they are not persuasive.

In the remarks, applicant argues in substance:

A: Lampaert does not teach identifying transistors in a sub-circuit configuration that includes respective interconnections linked to each of said transistors.

B: Lampeart does not teach physical verification.

C: Lampaert teaches away from checking the layout of a design against its schematic (LVS) representation, and how to actually perform this LVS check.

D: Lampaert does not teach measuring element electrical values from a circuit layout.

E: Lampeart does not teach comparing the measured parameters of each of said sub-circuits or the remaining step of claims 1 and 17; determining if all of said comparisons returns a correct correlation.

F: Li does not teach providing device model parameters that support an extraction of a list of device layout geometric parameters; and providing specific marker shapes to define the device layout geometric parameters.

G: Li does not disclose "providing device model parameters...." Especially a sub-circuit based device model which supports a complex layout extraction with a list of sub-circuit geometric parameters".

H: Li does not disclose wherein said devices are selected from ....compounded semiconductor transistors.

I: Li does not disclose wherein further marker shapes are added to non-FET devices.

J: Li does not disclose non-FET devices are selected from the group consisting of integrated on-chip inductors....

Examiner respectfully disagrees for the following reasons:

As to A: Lampaert does teach identifying transistors in a sub-circuit configuration that includes respective interconnections linked to each of said transistors [abstract, paragraph 0055, 0057, fig. 6 – in paragraph 0055, Lampaert discloses a sub-circuit

model which is used as a predictor of electrical behavior of MOSFETs among other thins such as layout v. schematic verification. Examiner contends that the use of such model for design processes inherently includes the identification of the RF MOSFET circuit elements as depicted in fig. 6 as a necessary part of using the model for design processes].

As to B: Lampaert does teach physical verification [fig. 8, element 810 – LVS, paragraphs 0055 disclose that a layout is generated as well as fig. 8 showing the generation of a layout and then LVS is done, Further, physical verification is only part of the preamble in the claim, and does not read into the body of the claim.].

As to C: Lampaert does not teach away from checking the layout of a design against its schematic (LVS) representation, and how to actually perform this LVS check [fig. 8, element 810 – LVS, paragraphs 0055 disclose that a layout is generated as well as fig. 8 showing the generation of a layout and then LVS is done. "How to actually perform this LVS check" is not a claimed, limitation.].

As to D: Lampaert does teach measuring element electrical values from a circuit layout [element electrical value are extracted (measured) from a circuit layout, paragraph 0056, "the layout generator interprets values from prior to generating a layout representation fig. 8, element 812, see also applicant remarks page 2, last paragraph where applicant discloses the extraction (measuring) part of the program].

As to E: Lampeart does teach comparing the measured parameters of each of said sub-circuits or the remaining step of claims 1 and 17; and determining if all of said comparisons returns a correct correlation [fig. 8, element 810 – the DRC and LVS

inherently compare the measured (extracted values from the generated layout) and determine if the returns are correct through the verification process];

As to F: Li does teach providing device model parameters that support an extraction of a list of device layout geometric parameters [paragraphs 0006-0008]; and providing specific marker shapes to define the device layout geometric parameters [paragraphs 0008, 0011, 0017, 0044-0046, the addition of the dummy or marker geometries at least defines layout parameters such as those needed for the correction of errors and for conforming to design rules].

As to G: The argument that Li does not disclose "providing device model parameters...." Especially a sub-circuit based device model which supports a complex layout extraction with a list of sub-circuit geometric parameters" is not relevant because it is not a claimed limitation.].

H: The argument that Li does not disclose wherein said devices are selected from ....compounded semiconductor transistors is moot since the rejection of record is removed.

I: Li does disclose wherein further marker shapes are added to non-FET devices paragraph 0043, where the IC devices may be devices other than FETs].

J: The argument that Li does not disclose non-FET devices are selected from the group consisting of integrated on-chip inductors.... Is moot since the rejection of record is removed.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW
April 14, 200